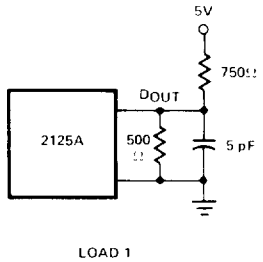
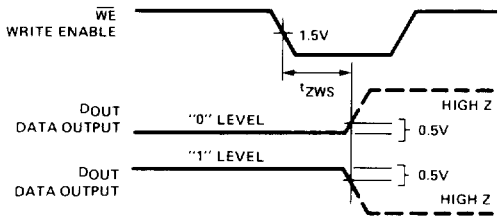
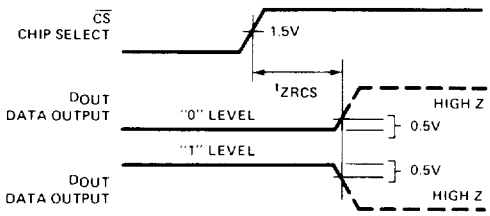
2125A FAMILY WRITE ENABLE TO HIGH Z DELAY



LOAD 1



2125A FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(ALL t_{ZXXX} PARAMETERS ARE MEASURED AT A DELTA OF 0.5V FROM THE LOGIC LEVEL AND USING LOAD 1.)

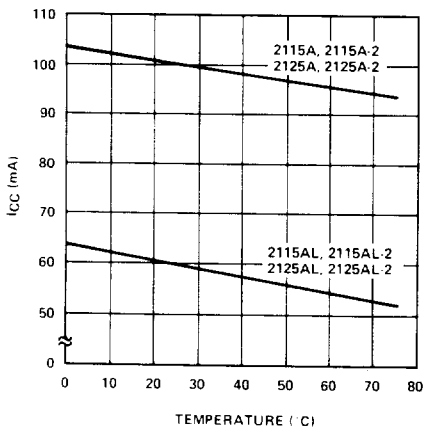
2115A/2125A FAMILY CAPACITANCE* V_{CC}= 5V, f = 1 MHz, T_A = 25°C

SYMBOL	TEST	2115A Family LIMITS		2125A Family LIMITS		UNITS	TEST CONDITIONS
		TYP.	MAX.	TYP.	MAX.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS}$ = 5V, All Other Inputs = 0V, Output Open

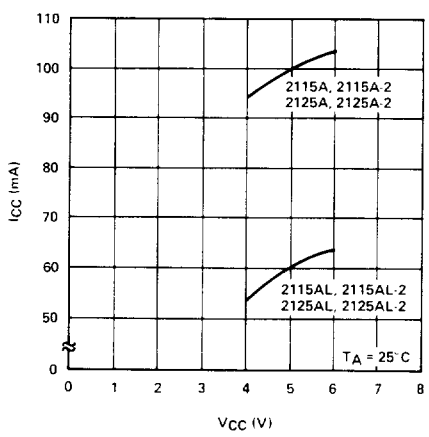
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

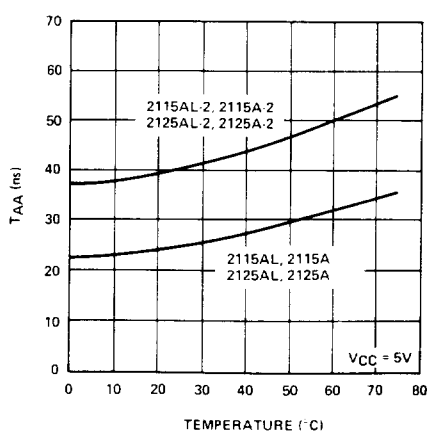
I_{CC} VS. TEMPERATURE



I_{CC} VS. V_{CC}



ACCESS TIME VS. TEMPERATURE



2125 FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

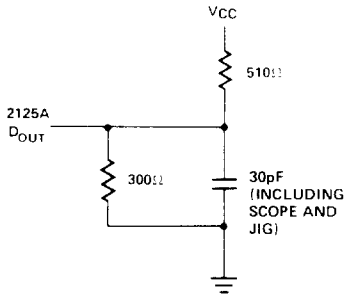
READ CYCLE

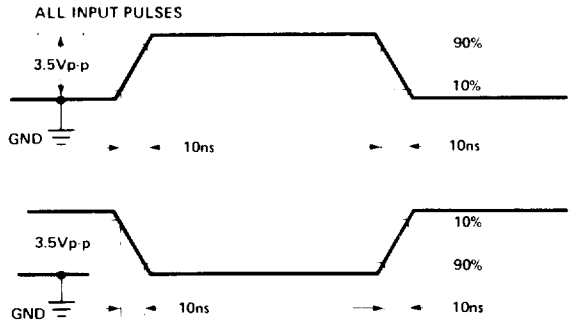
Symbol	Test	2125AL Limits Min.	Typ.	Max.	2125A Limits Min.	Typ.	Max.	2125AL-2 Limits Min.	Typ.	Max.	2125A-2 Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{ZRCS}	Chip Select to HIGH Z		10	30		10	30		10	30		10	40	ns
t_{AA}	**Address Access Time**		**30**	**45**		**30**	**45**		**40**	**70**		**40**	**70**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			10			ns

WRITE CYCLE

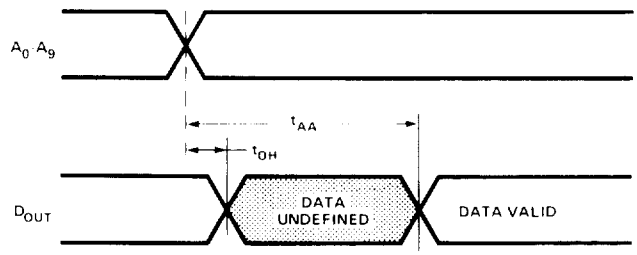
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z		10	25		10	30		10	25		10	40	ns
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	10		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

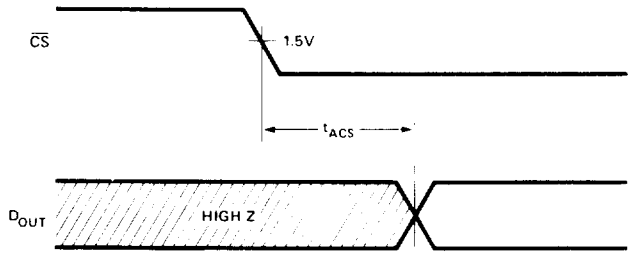




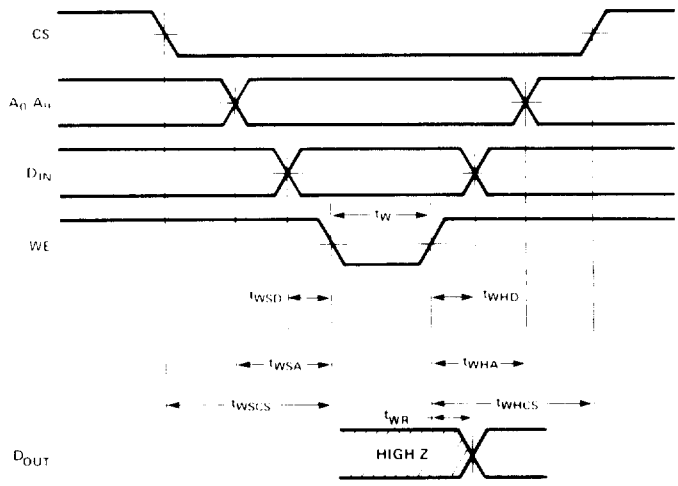
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

2115A FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

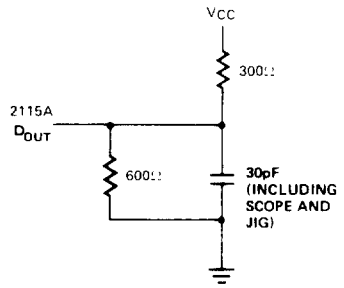
READ CYCLE

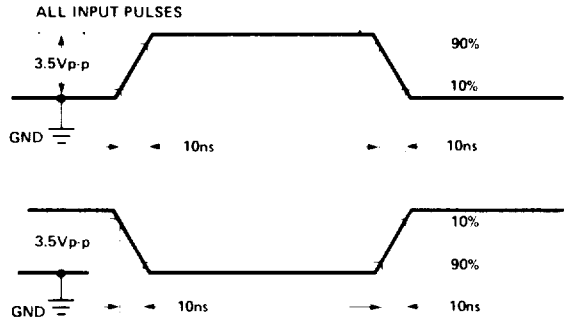
Symbol	Test	2115AL Limits Min.	Typ.	Max.	2115A Limits Min.	Typ.	Max.	2115AL-2 Limits Min.	Typ.	Max.	2115A-2 Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{RCS}	Chip Select Recovery Time		10	30		10	30		10	30		10	40	ns
t_{AA}	**Address Access Time**		**30**	**45**		**30**	**45**		**40**	**70**		**40**	**70**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			10			ns

WRITE CYCLE

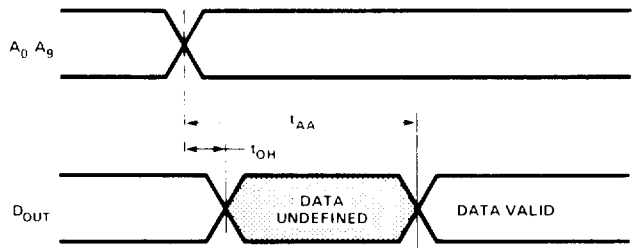
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time		10	25		10	30		10	25		10	40	
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	15		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

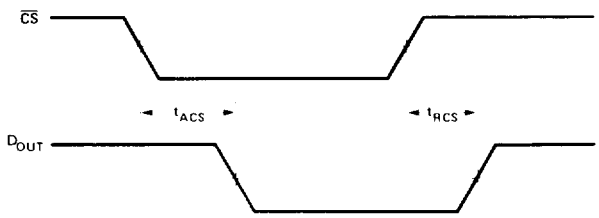




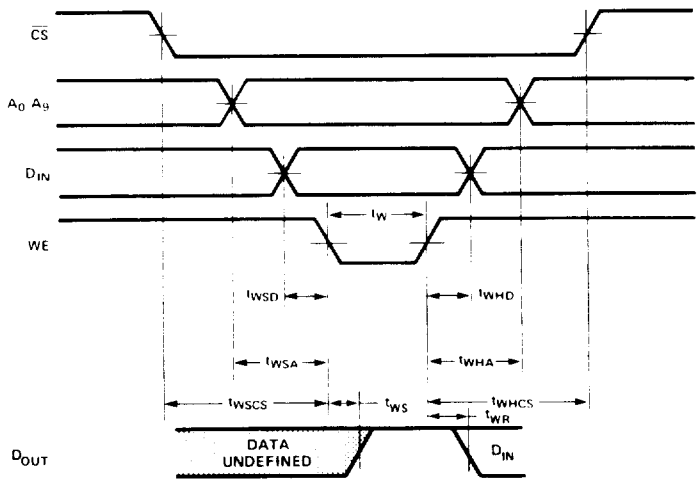
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . –10°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
All Output or Supply Voltages . . . . . –0.5V to +7V
All Input Voltages . . . . . –0.5V to +5.5V
D.C. Output Current . . . . . 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1,2]

V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	2115A Family Output Low Voltage			0.45	V	I_{OL} = 16 mA
V_{OL2}	2125A Family Output Low Voltage			0.45	V	I_{OL} = 7 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		–0.1	–40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	2115A Family Output Leakage Current		0.1	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	2125A Family Output Current (High Z)		0.1	50	μA	V_{CC} = Max., V_{OUT} = 0.5V/2.4V
I_{OS}[3]	2125A Family Current Short Circuit to Ground			–100	mA	V_{CC} = Max.
V_{OH}	Family Output High Voltage	2.4			V	I_{OH} = –3.2 mA
I_{CC}	Power Supply Current: I_{CC1}: 2115AL, 2115AL-2, 2125AL, 2125AL-2		60	75	mA	All Inputs Grounded, Output Open
	I_{CC2}: 2115A, 2115A-2, 2125A, 2125A-2		100	125	mA	

NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W

2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

2115A. 2125A FAMILY
HIGH SPEED 1K X 1 BIT STATIC RAM

	2115AL 2125AL	2115A 2125A	2115AL-2 2125AL-2	2115A-2 2125A-2
Max. T_{AA}(ns)	45	45	70	70
Max. I_{CC}(mA)	75	125	75	125

- **Pin Compatible To 93415A (2115A) And 93425A (2125A)**
- **Fan-Out Of 10 TTL (2115A Family) -- 16mA Output Sink Current**
- **Low Operating Power Dissipation --Max. 0.39mW/Bit (2115AL, 2125AL)**
- **TTL Inputs And Outputs**
- **Single +5V Supply**
- **Uncommitted Collector (2115A) And Three-State (2125A) Output**
- **Standard 16-Pin Dual In-Line Package**

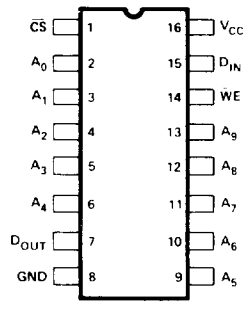
The Intel® 2115A and 2125A families are high-speed, 1024 words by 1 bit random access memories. Both open collector (2115A) and three-state output (2125A) are available. The 2115A and 2125A use fully DC stable (static) circuitry throughout — in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

The 2115AL/2125AL at 45 ns maximum access time and the 2115AL-2/2125AL-2 at 70 ns maximum access time are fully compatible with the industry-produced 1K bipolar RAMs, yet offer a 50% reduction in power of their bipolar equivalents. The power dissipation of the 2115AL/2125AL and 2115AL-2/2125AL-2 is 394 mW maximum as compared to 814 mW maximum of their bipolar equivalents. For systems already designed for 1K bipolar RAMs, the 2115A/2125A and the 2115A-2/2125A-2 at 45 ns and 70 ns maximum access times, respectively, offer complete compatibility with a 20% reduction in maximum power dissipation.

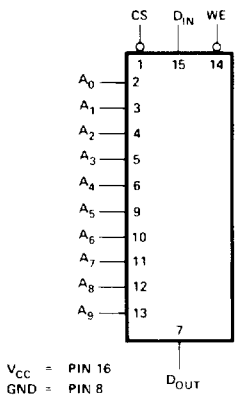
The devices are directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

The 2115A and 2125A families are fabricated with Intel's N-channel MOS Silicon Gate Technology.

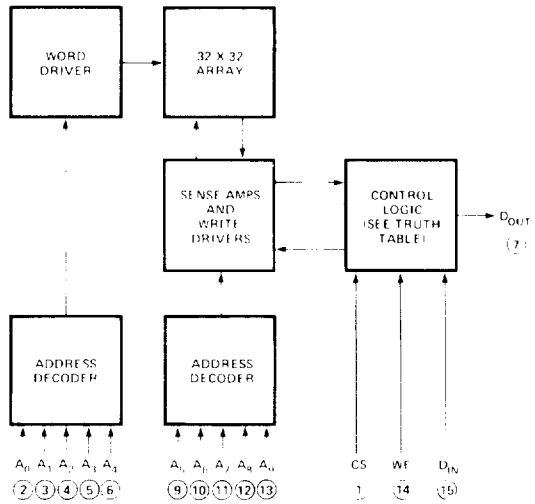
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

TRUTH TABLE

INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
CS	WE	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ